


GA-78LMT-USB3

Revision :6.01

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| 21 | REALTEK ALC892 |
| 22 | RGB ,COM ,LPT ,F_USB ,FAN |
| 23 | ITE 8620 _KB/MS_HWM |
| 24 | ATX, FRONT PANEL |
| 25 | VCORE(RT8868+RT9612) |

[illegible]

| | | | | |
|---|--------------------------|-------|---------|------|
|  | | | | |
| Title | | | | |
| <div>COVER SHEET</div> | | | | |
| Size | Document Number | | | Rev |
| Custom | GA-78LMT-USB3 | | | 6.01 |
| Date: | Friday, October 31, 2014 | Sheet | 1 of 31 | |

Model Name:GA-78LMT-USB3

Version: 6.01

BOM : 9M78LTUB3-00
P-Code: U99098-0

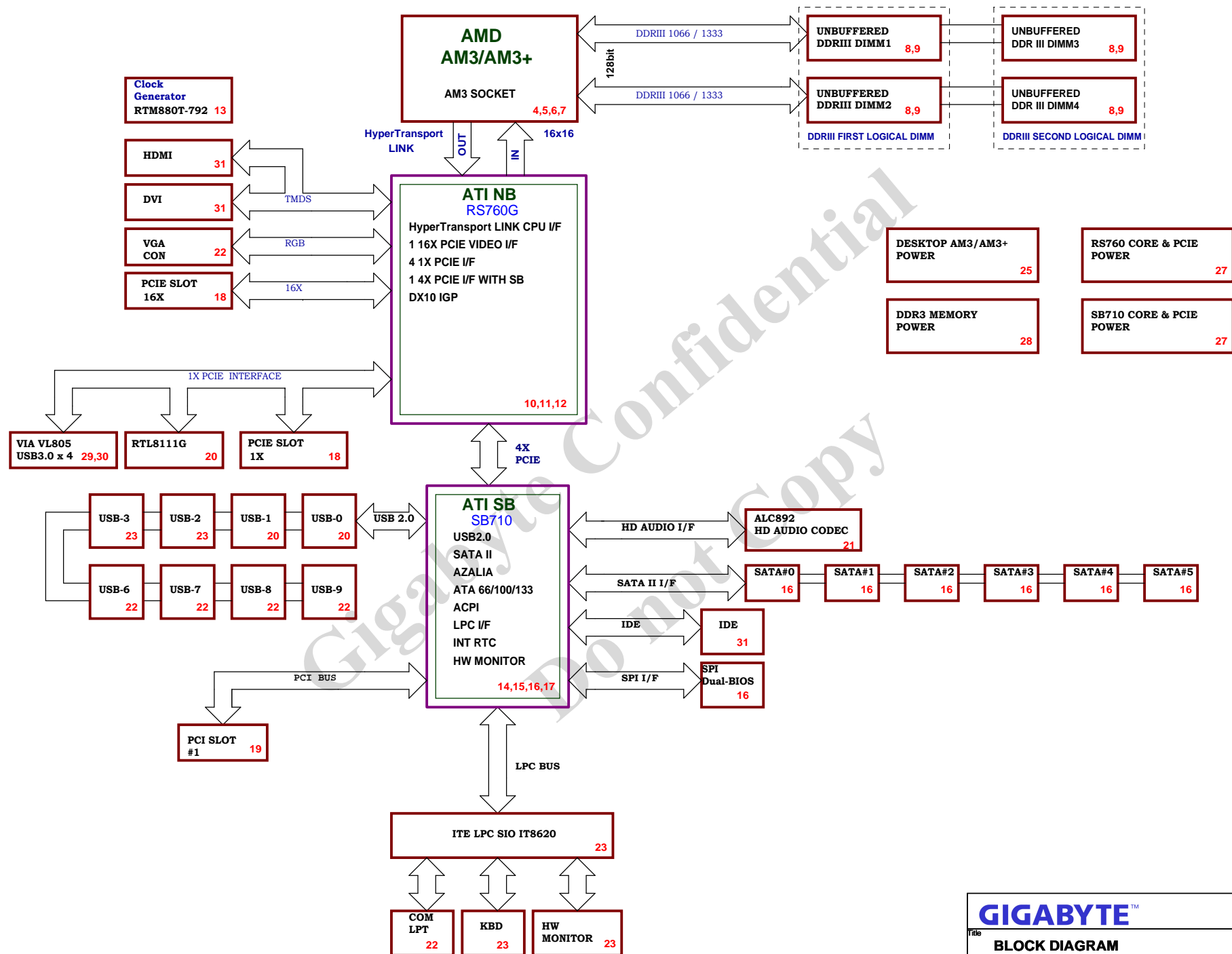
Component value change history

[illegible]

Circuit or PCB layout change for next version

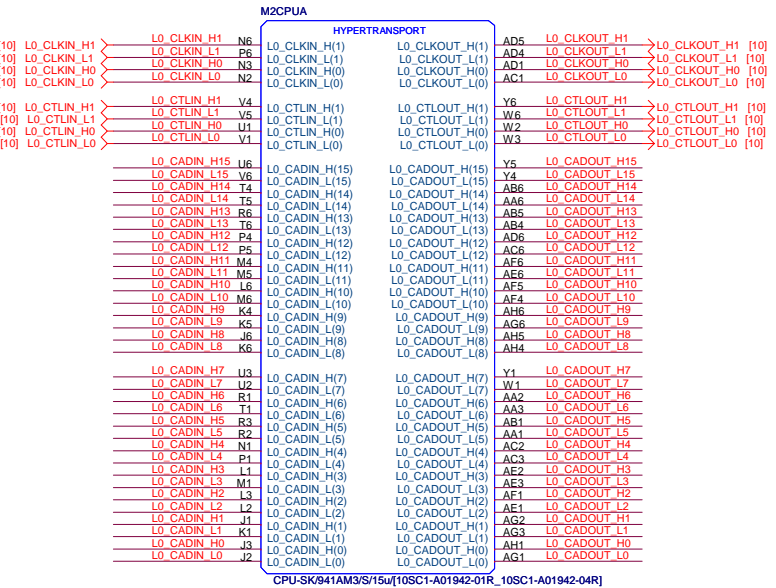
[illegible]

RS780L CUSTOMER DESKTOP DESIGN



L0_CADIN_L[0..15] L0_CADIN_L[0..15] [10]
L0_CADIN_H[0..15] L0_CADIN_H[0..15] [10]

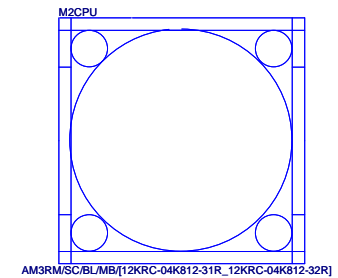
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L0_CADOUT_H[0..15] L0_CADOUT_H[0..15] [10]

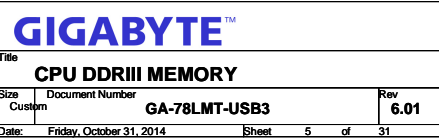


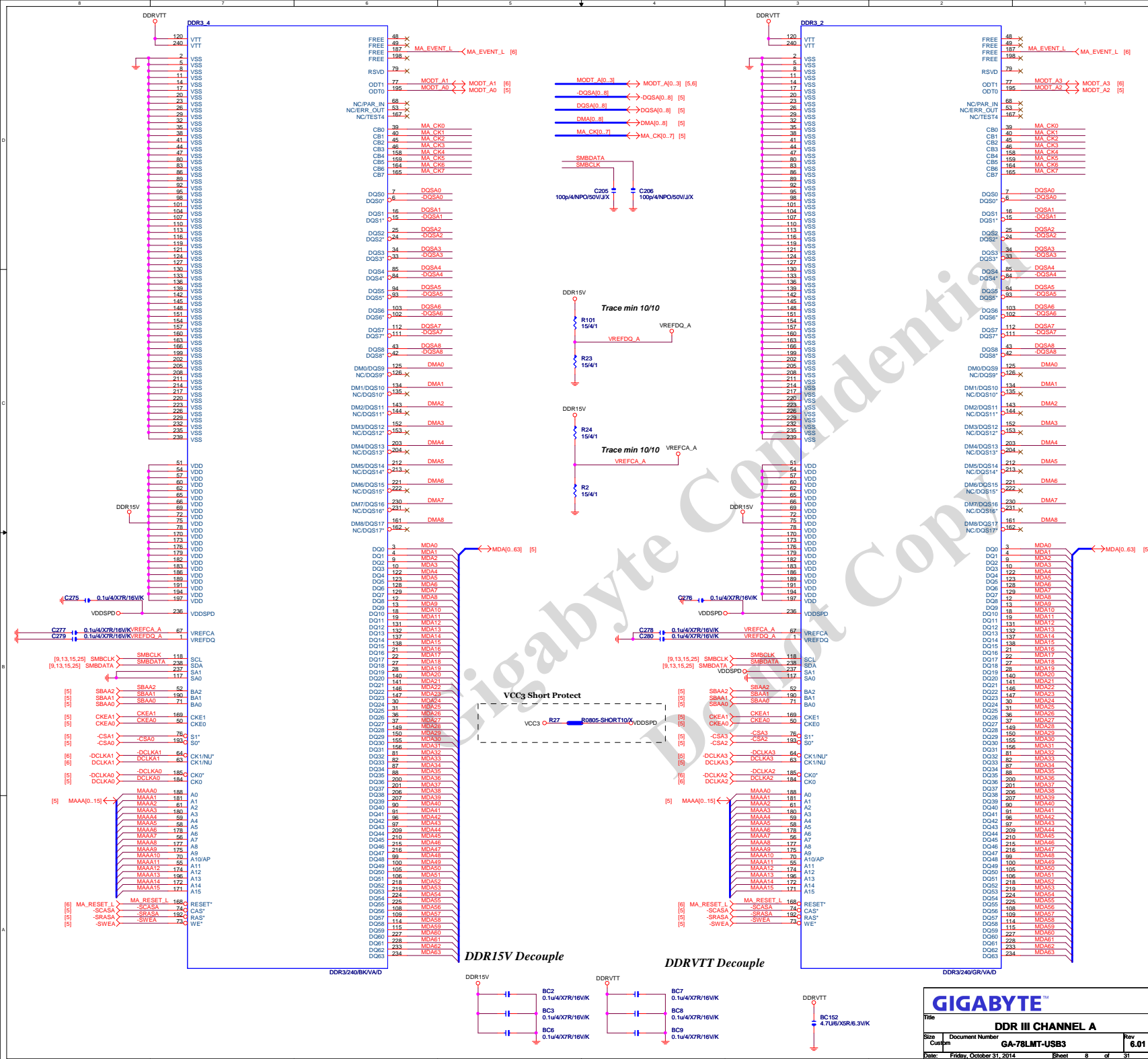
Gigabyte Confidential
Do not Copy

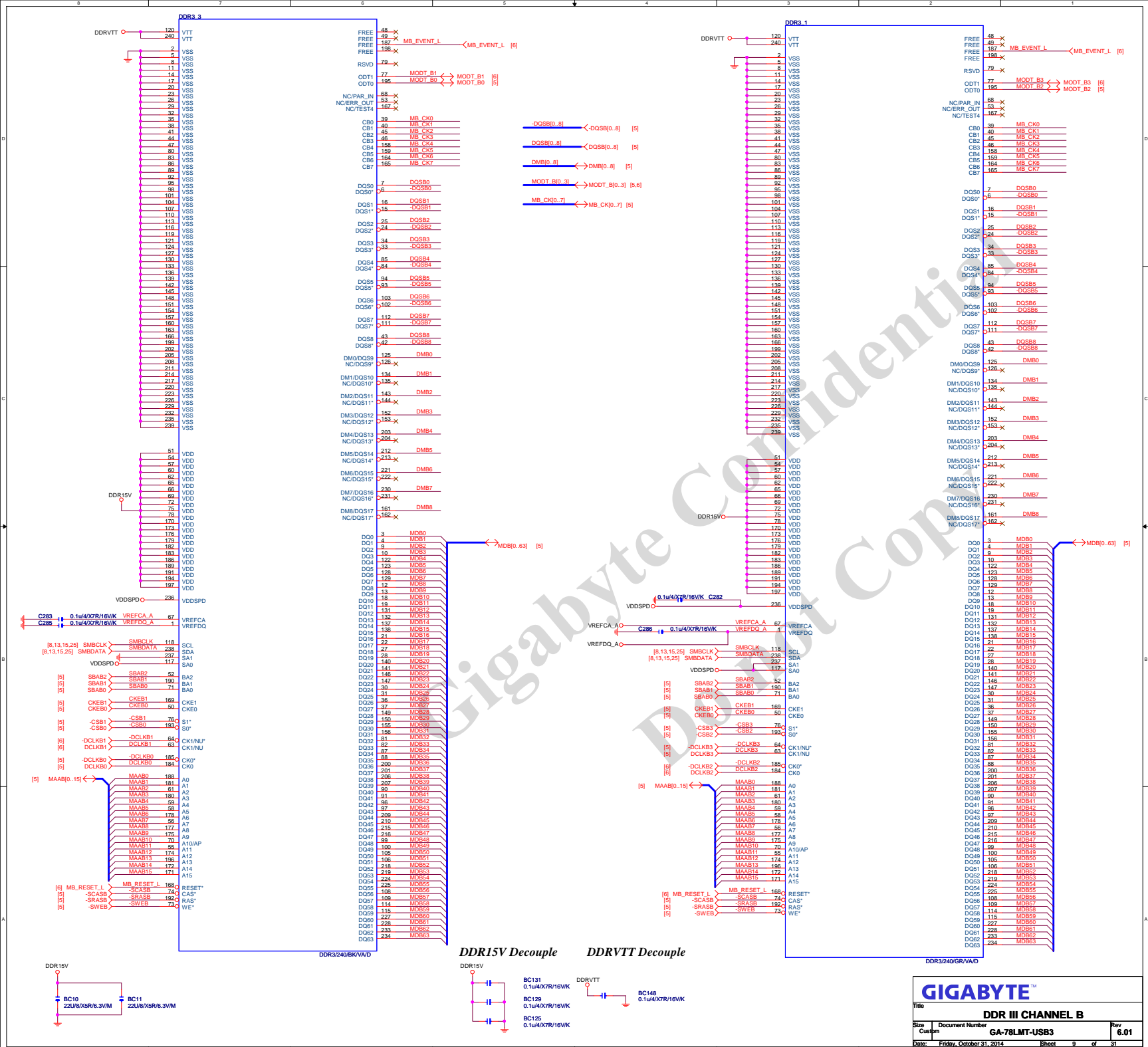
CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR18V
CPU_VTT_SUS = DDRVTT

VLDT_A = VCC12_HT
VLDT_B = HT12B









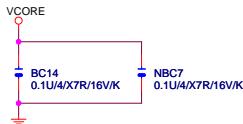
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L0_CADIN_H[0..15] <L0_CADIN_H[0..15] [4]

L0_CADOUT_L[0..15] <L0_CADOUT_L[0..15] [4]
L0_CADOUT_H[0..15] <L0_CADOUT_H[0..15] [4]

U3A

PART 1 OF 6

HYPER TRANSPORT CPU I/F



EXP_A_RXP[0..15] >> EXP_A_RXP[0..15] [18]
EXP_A_RXN[0..15] >> EXP_A_RXN[0..15] [18]
EXP_A_TXP[0..15] >> EXP_A_TXP[0..15] [18]
EXP_A_TXN[0..15] >> EXP_A_TXN[0..15] [18]

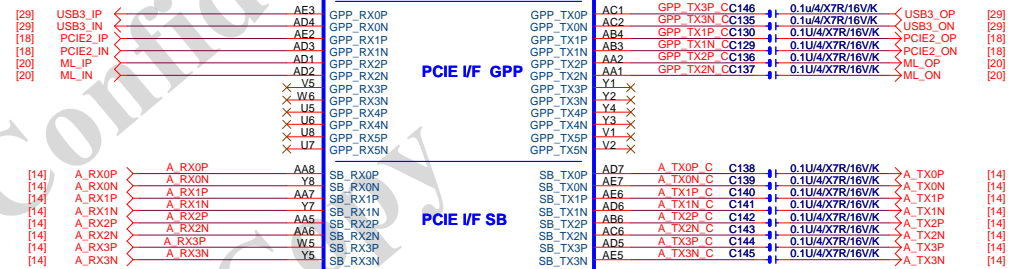
U3B

PART 2 OF 6

PCIE I/F GFX

PCIE I/F GPP

PCIE I/F SB



PCE_CALRP(PCE_BCALRP)
PCE_CALRN(PCE_BCALRN)

RS780L/FCBGA528/A13/[10HB1-06760G-20R]

NB_HS[12SP2-SA0701-11R_12SP2-SA0701-12R_12SP2-SA0701-13R]

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| Title | | |
|-------------------|--------------------------|----------------|
| RS780 HT-LINK I/F | | |
| Size | Document Number | Rev |
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| Date: | Friday, October 31, 2014 | Sheet 10 of 31 |

Note: for RS780, change R232 to 150R as AUX_CAL,
place close to pin C8

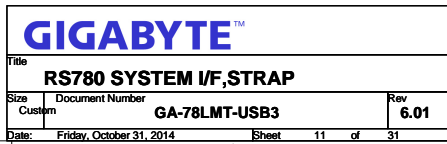
[22] DAC_VSYNC << R276 3K/4/1 VCC3

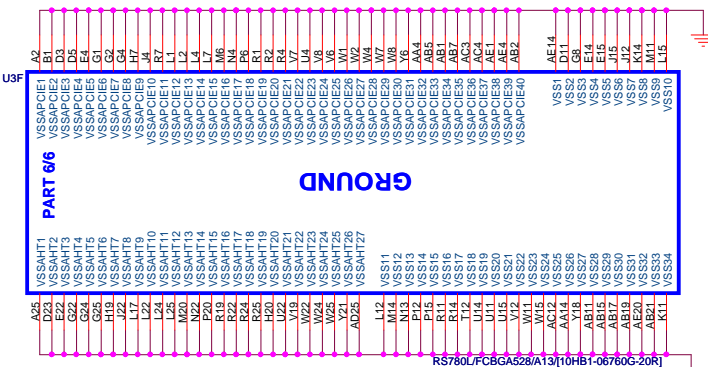
Note: for RX780, change following
pull-down resistor to 3K accordingly

R913 (RX780_DFT_GPIO4)
R218 (RX780_DFT_GPIO3)
R911 (RX780_DFT_GPIO2)

[22] DAC_HSYNC << R285 3K/4/1 VCC3

Note: for RX780, change following pull-down resistor to 3K accordingly
R219 (RX780_DFT_GPIO0)

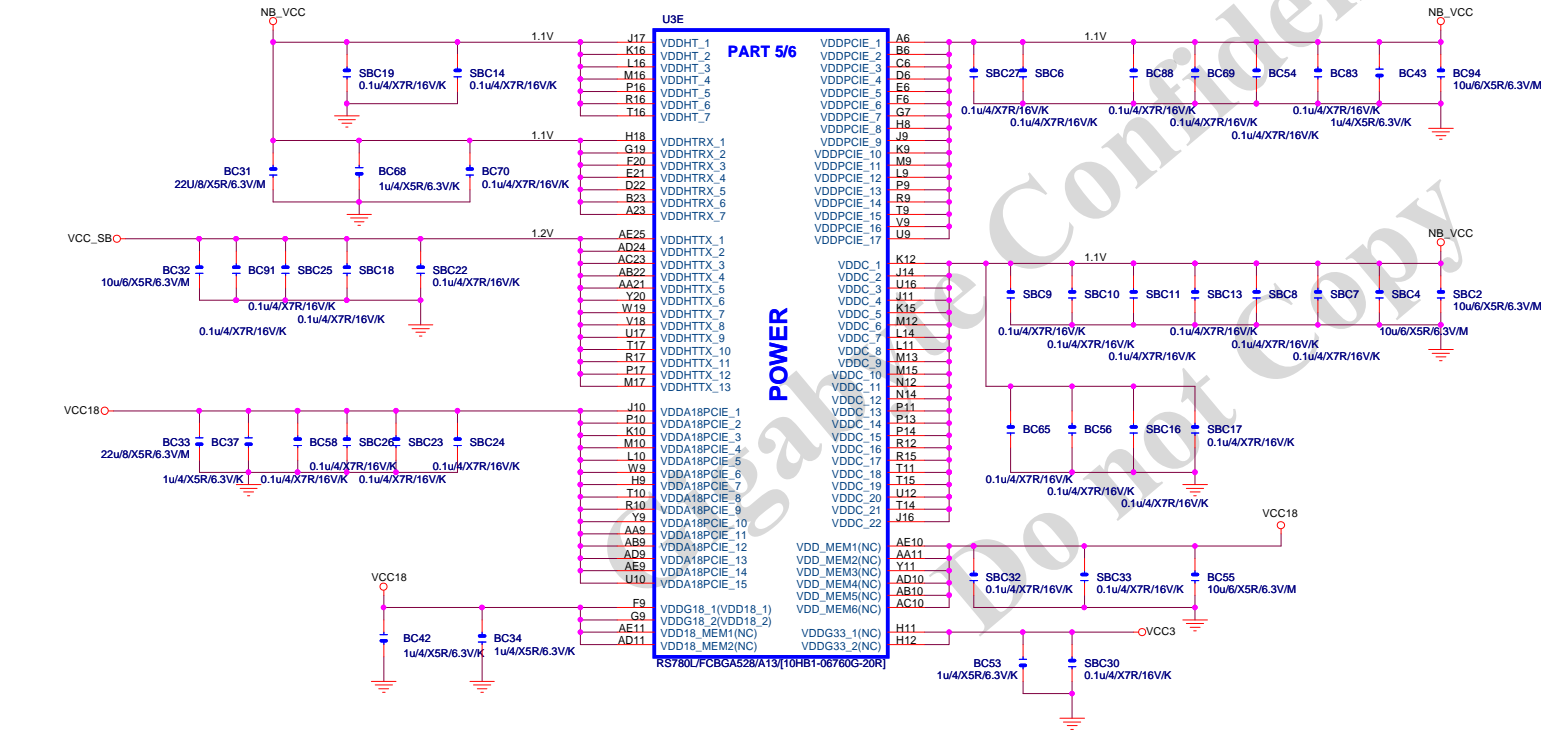


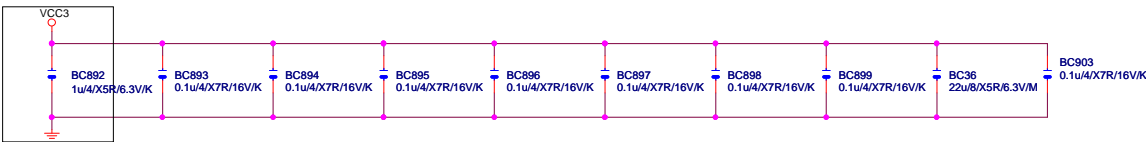


Please use 1mm pad size,
place all ELT test pads
on bottom side only

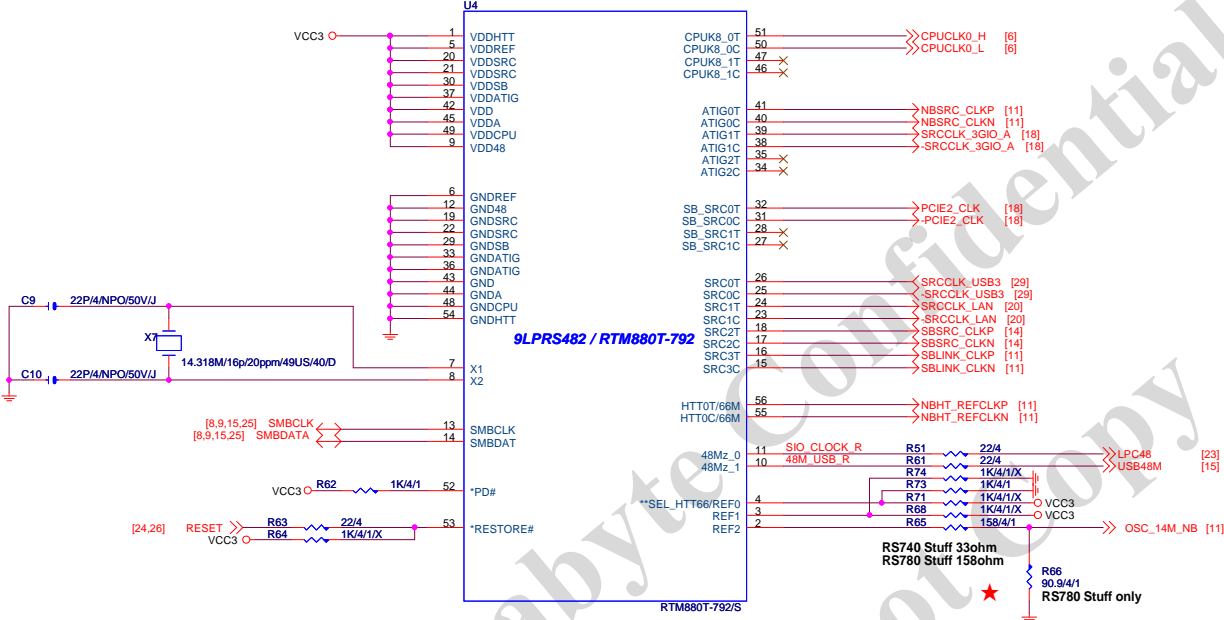
RS740/RX780/RS780 POWER DIFFERENCE TABLE

| PIN NAME | RS740 | RX780 | RS780 | PIN NAME | RS740 | RX780 | RS780 |
|------------|-------|-------|----------------------------|---------------|-------|-------|-------|
| VDDHT | NC | +1.1V | +1.1V | IOPLLVD | +1.2V | NC | +1.1V |
| VDDHTRX | NC | +1.1V | +1.1V | AVDD | +3.3V | NC | +3.3V |
| VDDHTTX | +1.2V | +1.2V | +1.2V | AVDDI | +1.8V | NC | +1.8V |
| VDDA18PCIE | NC | +1.8V | +1.8V | AVDDQ | +1.8V | NC | +1.8V |
| VDD18 | +1.8V | +1.8V | +1.8V | PLLVD | +1.2V | NC | +1.1V |
| VDD18_MEM | NC | NC | +1.8V | PLLVD18 | +1.8V | NC | +1.8V |
| VDDPCIE | +1.2V | +1.1V | +1.1V | VDDA18PCIEPLL | +1.2V | +1.8V | +1.8V |
| VDDC | +1.2V | +1.1V | +1.1V | VDDA18HTPLL | +1.8V | +1.8V | +1.8V |
| VDD_MEM | +1.8V | NC | +1.8V(DDR2) +1.5V(DDR3) | VDDLTP18 | +1.8V | NC | +1.8V |
| VDD33 | +3.3V | NC | +3.3V | VDDLTP18 | +1.8V | NC | +1.8V |
| IOPLLVD18 | +1.8V | NC | +1.8V | VDDLTP18 | +1.8V | NC | +1.8V |





- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE
- 2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN



watch dog --
RESTORE# 接 RESET

| | |
|----------------------|-----------------|
| | OSC_14M_NB |
| RS740 | 3.3V 33R serial |
| RX780 | 1.8V 82.5R/130R |
| RS780 (Single-ended) | 1.1V 158R/90.9R |

| | | |
|------------------|------|--|
| **SEL_HTT66/REF0 | | OUT 3.3V 14.318MHz REF output. |
| IN | Low | 100MHz differential HT clock, (Internal 120KΩ pull-down) |
| | High | 66MHz 3.3V single ended HT clock. |

| NB CLOCKS | RS740 | RX780 | RS780 | |
|--------------|---------------|---------------|----------------|-----------|
| HT_REFCLKP | 66M SE(SE) | 100M DIFF | 100M DIFF | |
| HT_REFCLKN | NC | 100M DIFF | 100M DIFF | |
| REFCLK_P | 14M SE (3.3V) | 14M SE (1.8V) | 14M SE (1.1V) | 100M DIFF |
| REFCLK_N | NC | NC | vref | 100M DIFF |
| GFX_REFCLK* | 100M DIFF | 100M DIFF | 100M DIFF | 100M DIFF |
| GPP_REFCLK | NC | 100M DIFF | 100M DIFF(OUT) | |
| GPPSB_REFCLK | 100M DIFF | 100M DIFF | 100M DIFF | |

* the GFX_REFCLK input is required for all cases

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Title

RTM880T-792

Size

Custom

Document Number

GA-78LMT-USB3

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6.01

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Friday, October 31, 2014

Sheet

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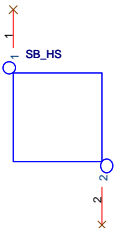
of

31

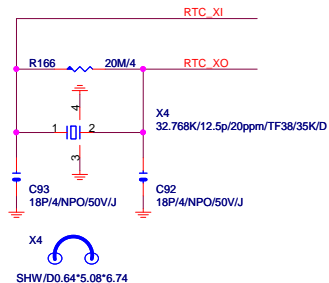


PLACE THESE PCIE AC COUPLING
CAPS CLOSE TO U600

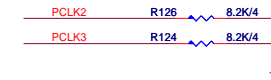
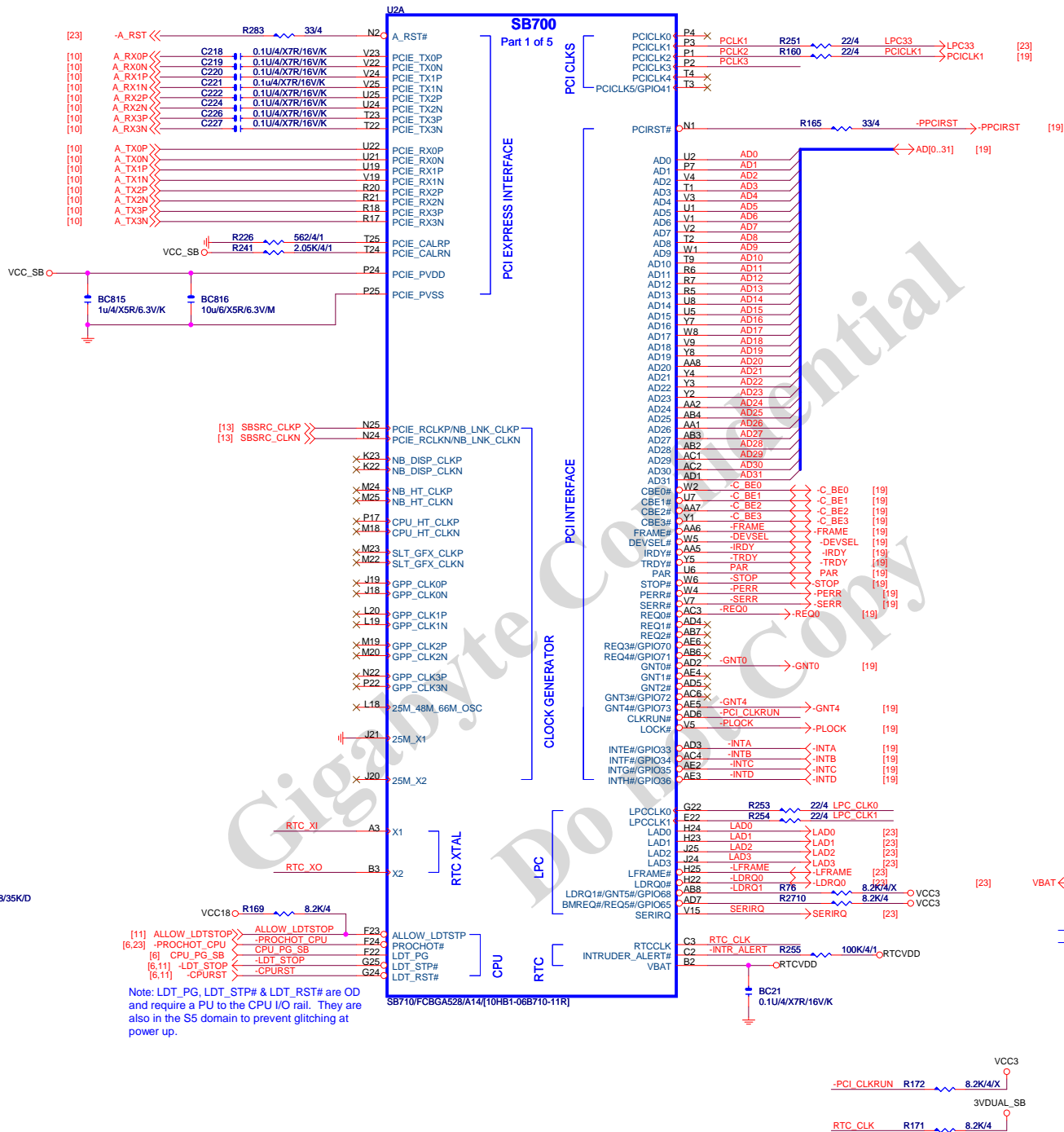
S.B HEATSINK



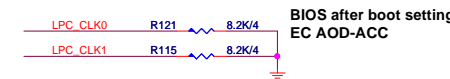
SB_HS[12SP2-030005-42R_12SP2-030005-43R]



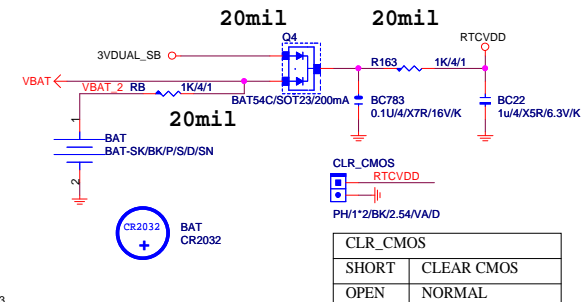
Note: LDT_PG, LDT_STP# & LDT_RST# are OD
and require a PU to the CPU I/O rail. They are
also in the S5 domain to prevent glitching at
power up.



| | PCLK2 | PCLK3 |
|-----------|--|--------------------------------------|
| PULL HIGH | WATCHDOG TIMER ON NB_PWRGD ENABLED | USE DEBUG STRAPS |
| PULL LOW | WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT | IGNORE DEBUG STRAPS DEFAULT |



| | LPC_CLK0 | LPC_CLK1 |
|-----------|-------------------------------|-------------------------------|
| PULL HIGH | IMC ENABLED AOD Extreme | CLKGEN ENABLED |
| PULL LOW | IMC DISABLED DEFAULT | CLKGEN DISABLED DEFAULT |



| CLR_CMOS | |
|----------|------------|
| SHORT | CLEAR CMOS |
| OPEN | NORMAL |

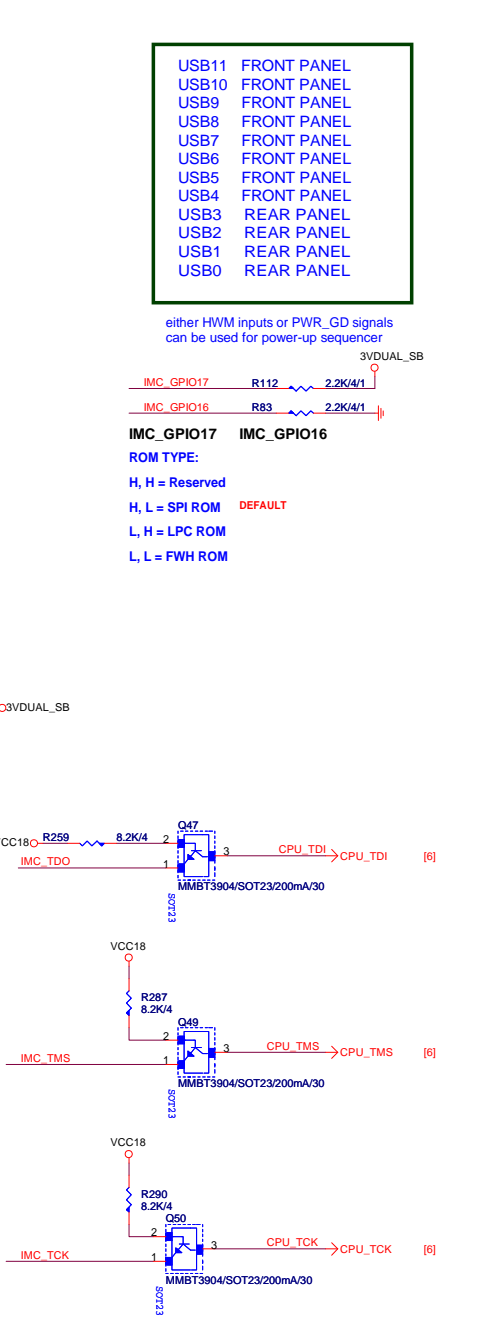
NOT ADD ICT FOR RTCVDD PIN

GIGABYTE™

ATI SB710 PCIE/PCI/CPU/LPC/CLK

| | | |
|--------|-----------------|------|
| Size | Document Number | Rev |
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| | | | | | |
|-------|--------------------------|-------|----|----|----|
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|-------|--------------------------|-------|----|----|----|

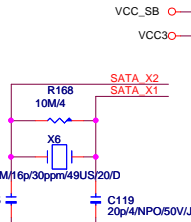
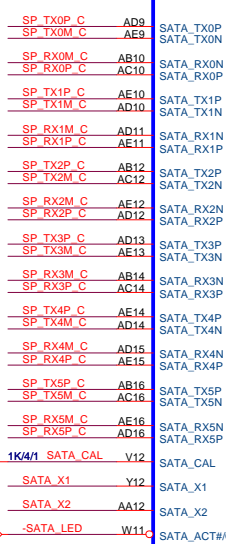




PLACE SATA AC COUPLING
CAPS CLOSE TO SB800

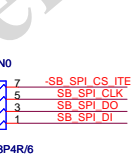
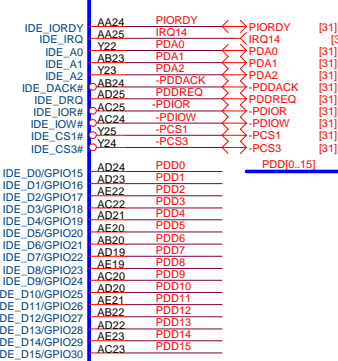
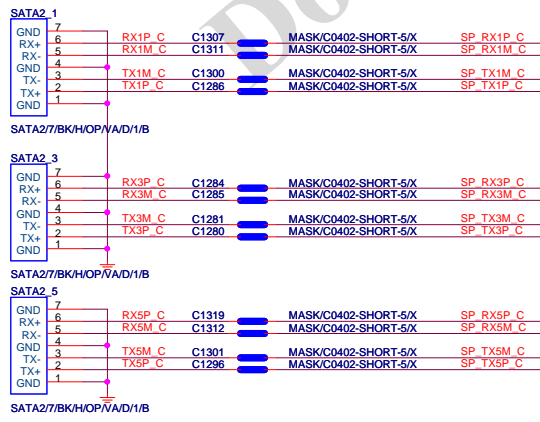
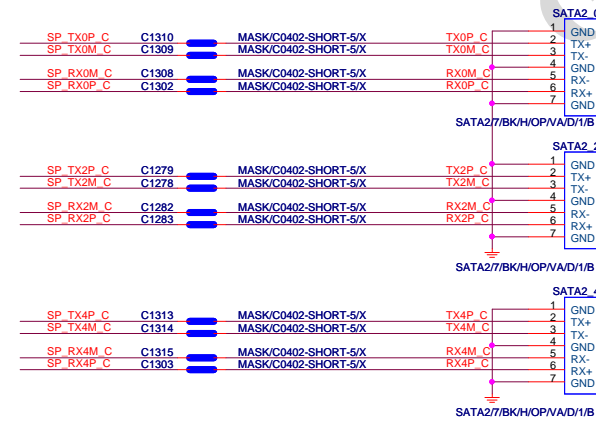
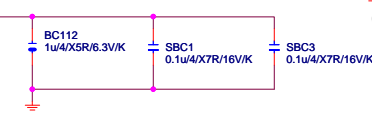
SB700

Part 2 of 5

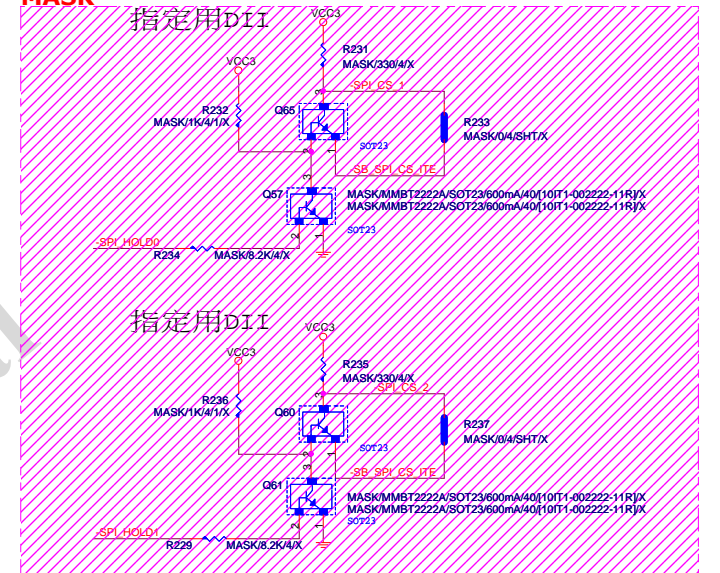


PLACE SATA_CAL
RES VERY CLOSE
TO BALL OF U600

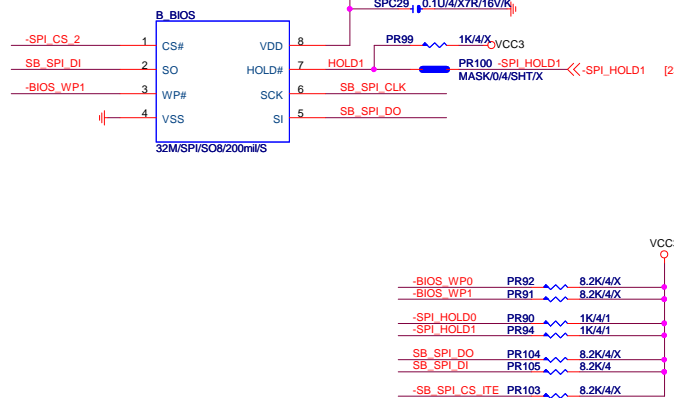
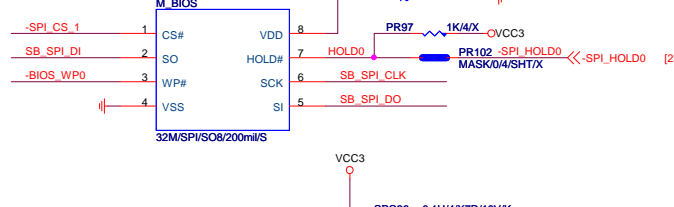
NOTE:
R650 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK

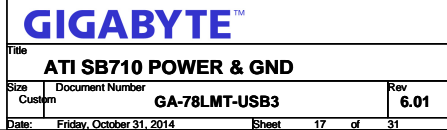


MASK



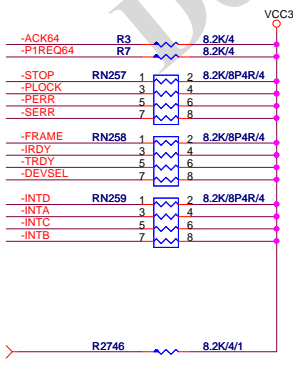
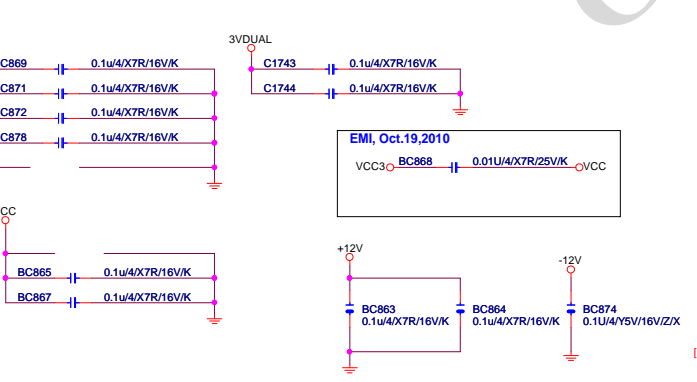
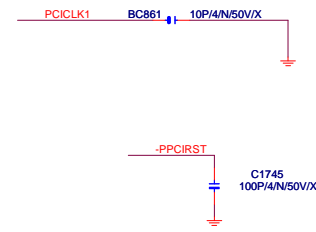
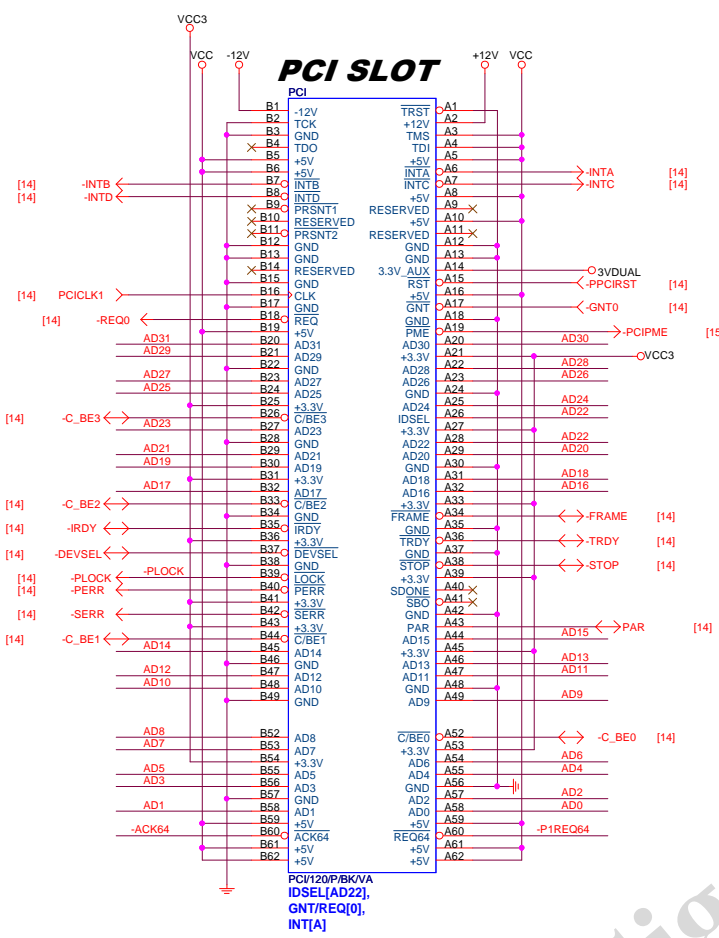
CHECK





PCI SLOT 1,2

[14] AD[0..31] <--> AD[0..31]



PCI SLOT

Size: Custom

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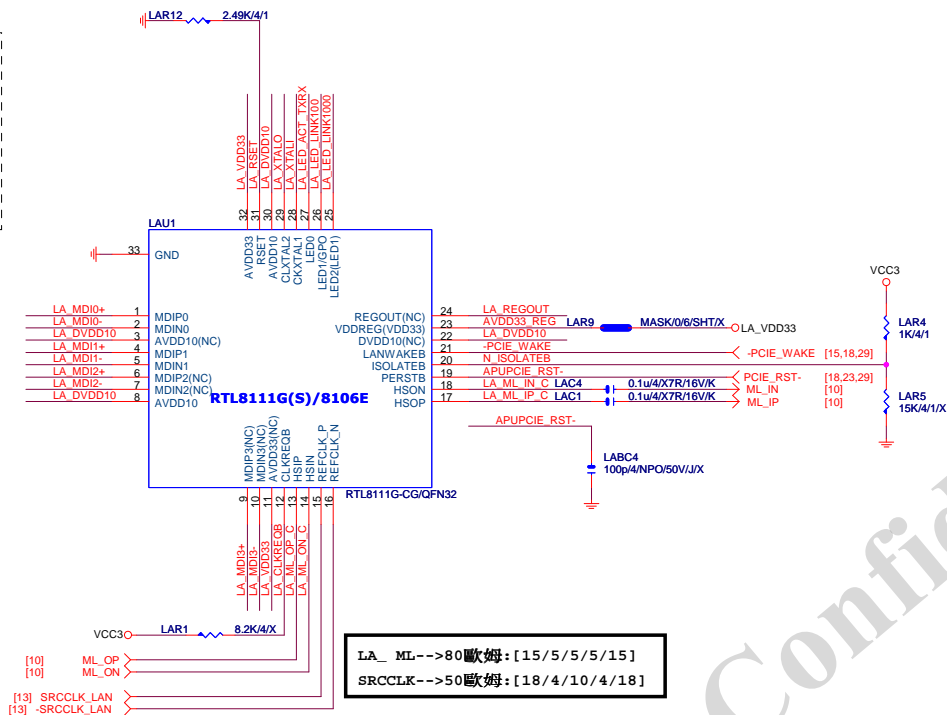
LAX1
25M/16p/30ppm/49US/20/D

LA.XTALI

LA.XTALO

LAC5
20p/4/NPO/50V/J

LAC6
20p/4/NPO/50V/J



(CLOSE LAU1 PIN22,30,3,8)

PIN22
LABC2
1u4/X5R/6.3V/K

PIN30
LABC9
0.1u4/X7R/16V/K

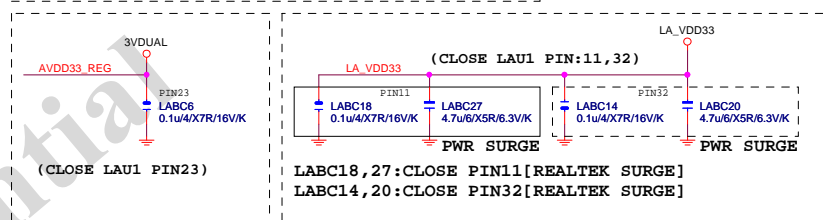
PIN3
LABC3
0.1u4/X7R/16V/K

PIN8
LABC8
0.1u4/X7R/16V/K

LA_DVDD10

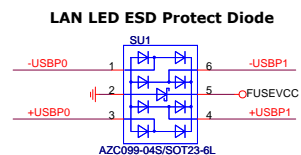
LABC2:1U CLOSE PIN22[REALTEK REQ]

```
| LABC2:1U CLOSE PIN22[REALTEK REQ]
```



NOTE:
RT8106E:PIN3,11,22,24-->NC
LABC2LABC3,LABC5,LABC18,LABC27-->N/A

5VDUAL ○ F6 SPR-P260T/6V/8/S ○ FUSEVCC



LAESD2

LA_MDI1- 1 6 LA_MDI1+

2 5 0.5V DUAL

LA_MDI0+ 3 4 LA_MDI0-

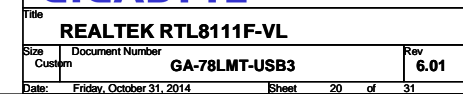
AZC099-04S/SOT23-6L/X

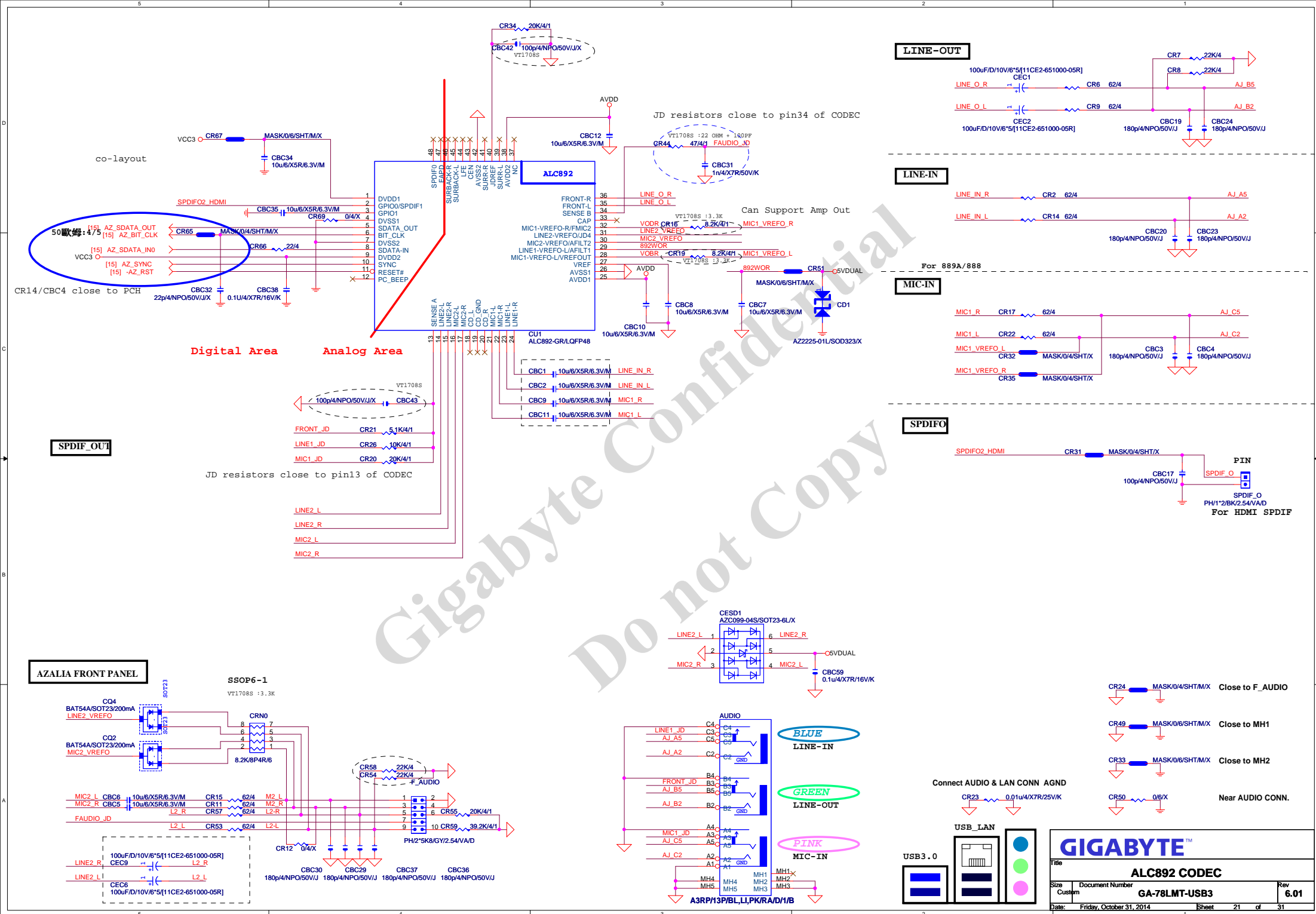
| 料號 | 規格 | 廠商 |
|-------------------------------|-----------------|---------------|
| 11NR6-702009-96R | 1G LAN (12core) | UDE(RU9 ESD+) |
| [LED獨立走線,可省略外加AZC099料件LAESD1] | | |

1. 9KV ESD BOM:
USB_LAN (RU9):11NR6-702009-96R
2. 28KV ESD BOM:
USB_LAN (RU9):11NR6-702009-96R
LAESD2,LAESD3:1件AZC398-04S

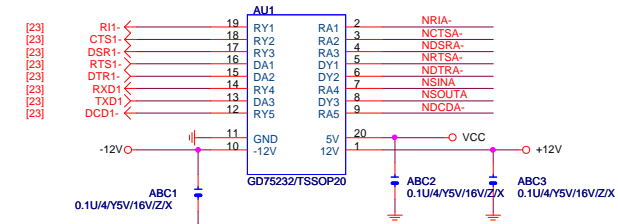
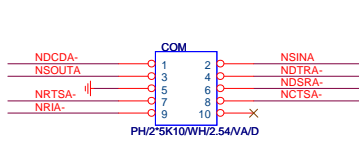
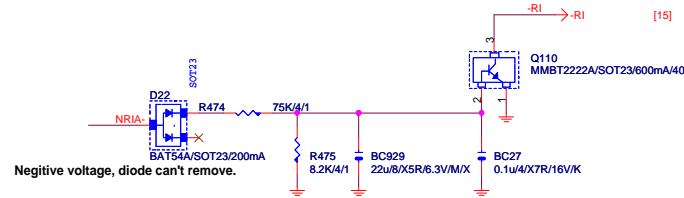
Between AUDIO & USB_LAN

Between USB_LAN & USB30

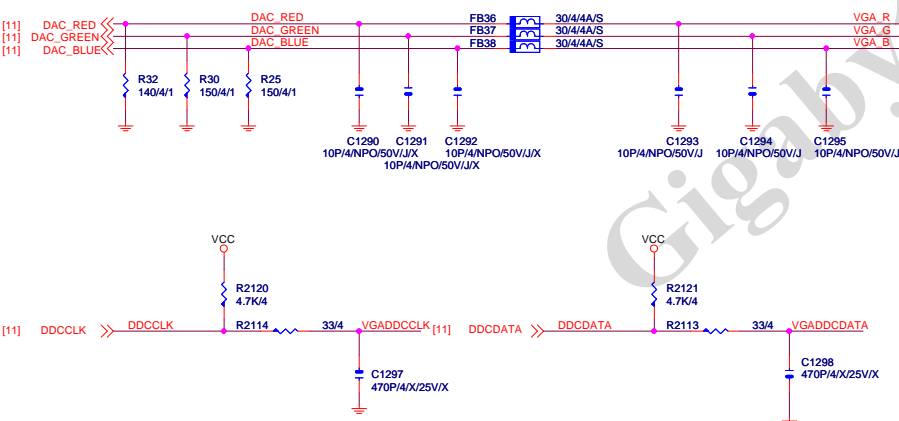
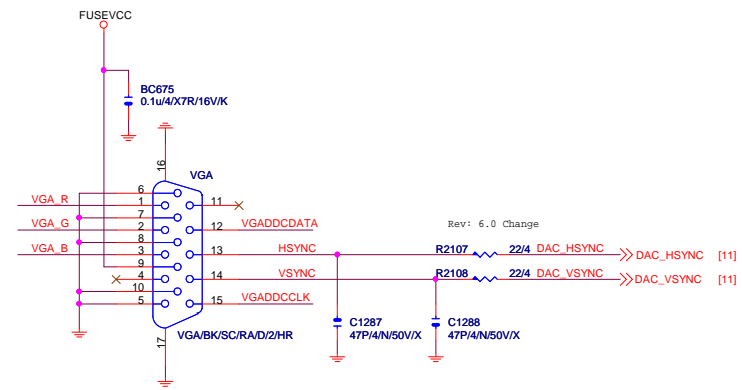




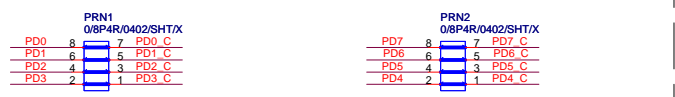
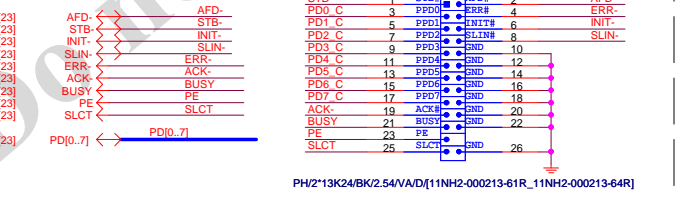
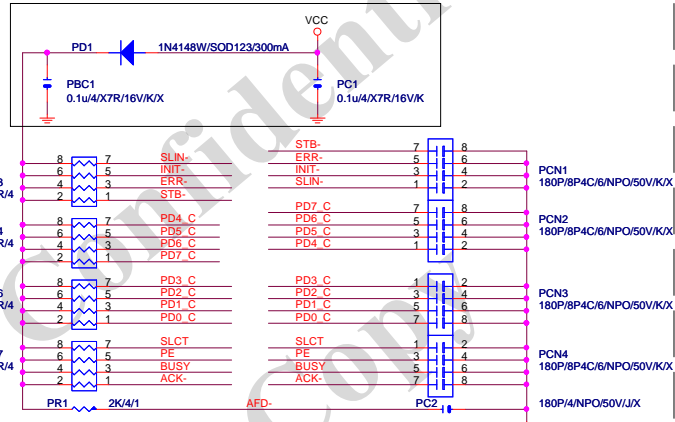
COM



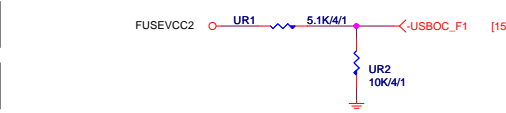
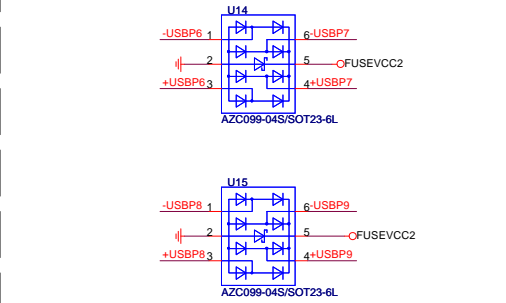
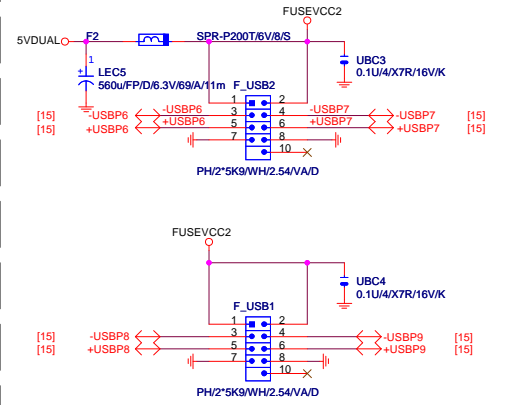
VGA

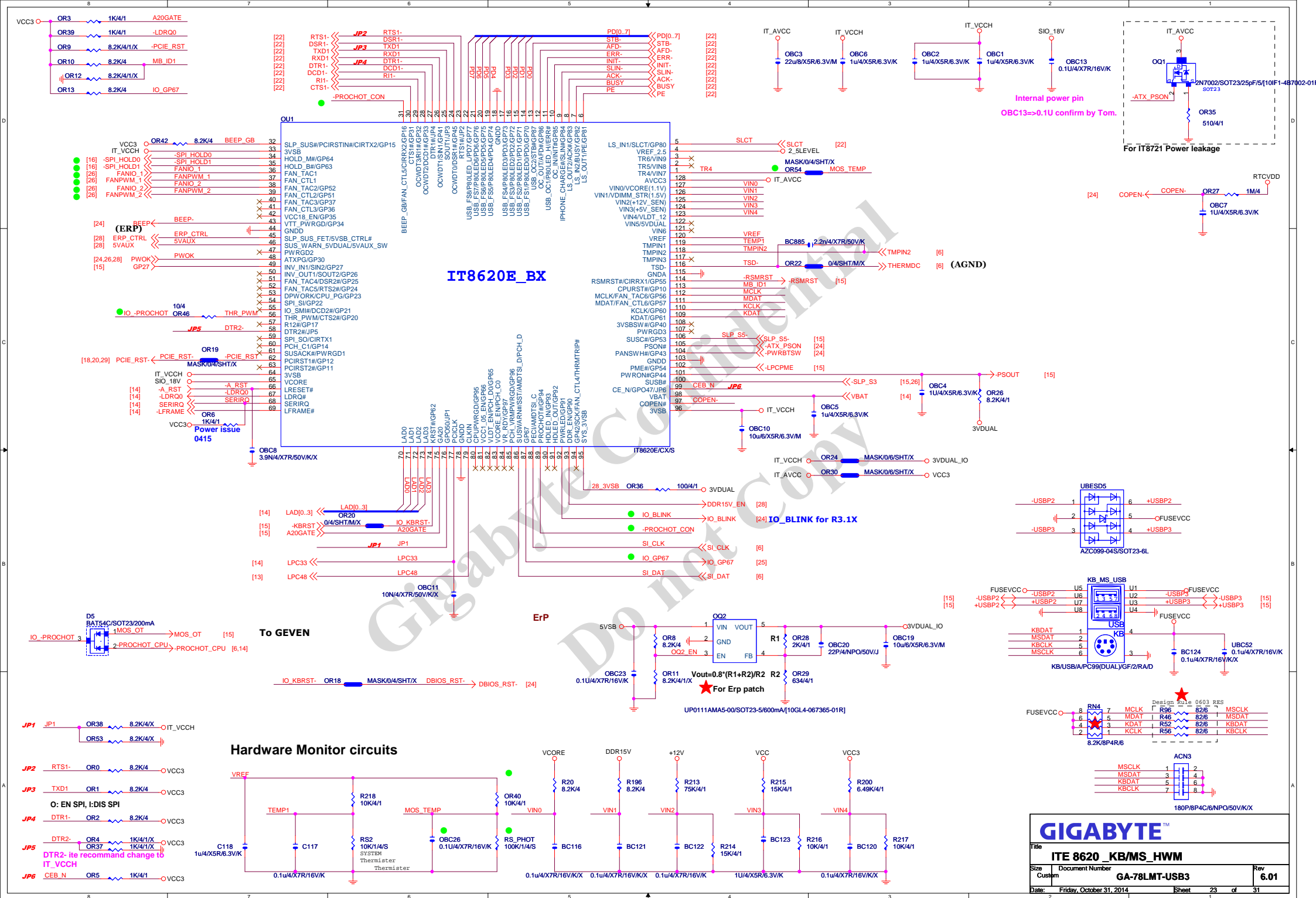


LPT

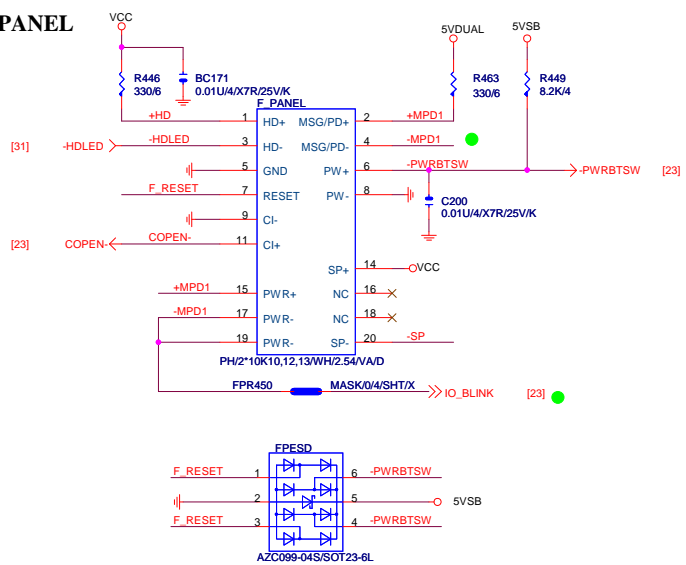


USB 2.0

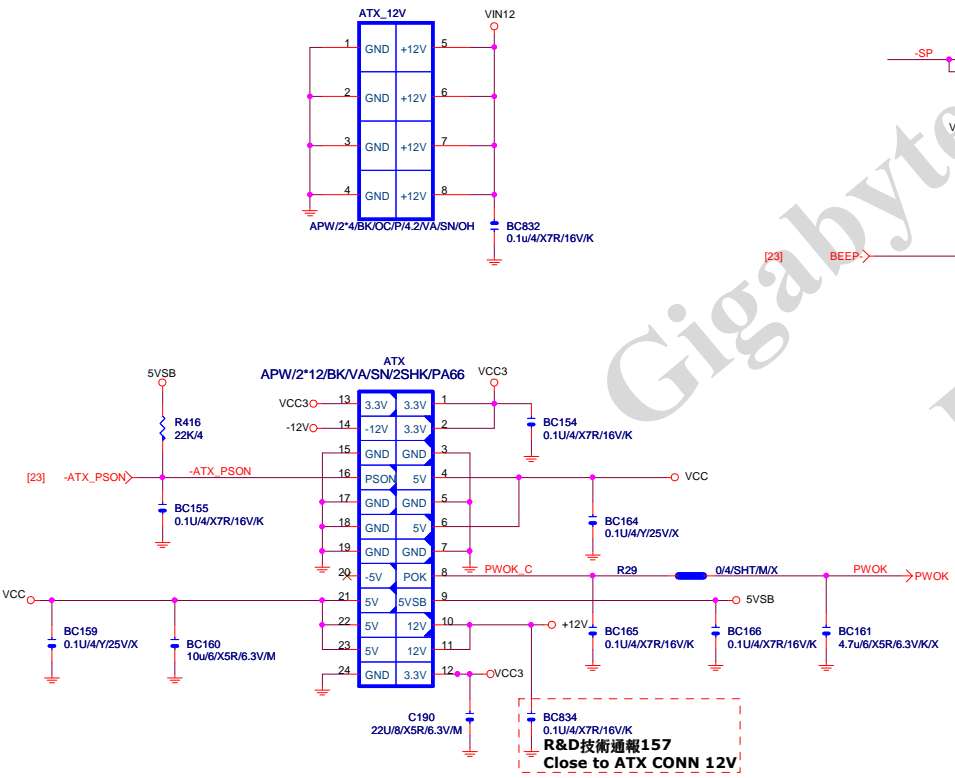




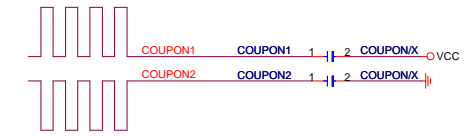
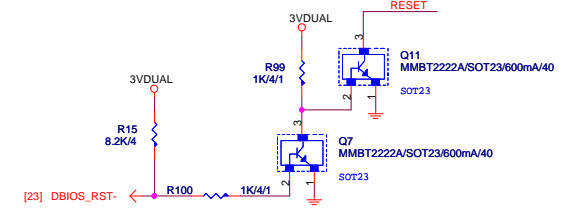
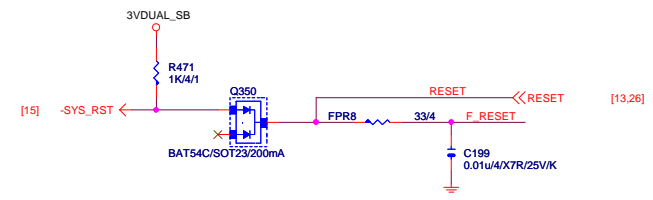
FRONT PANEL



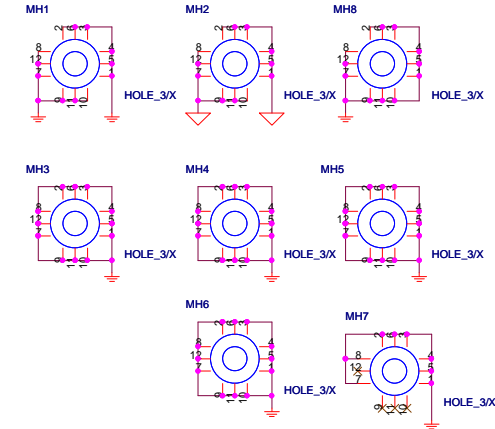
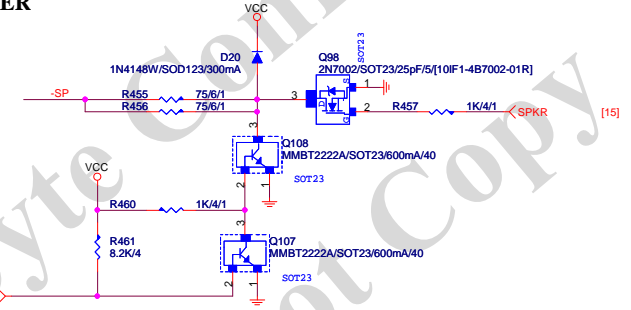
ATX POWER CONNECTOR



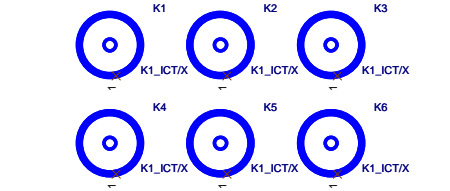
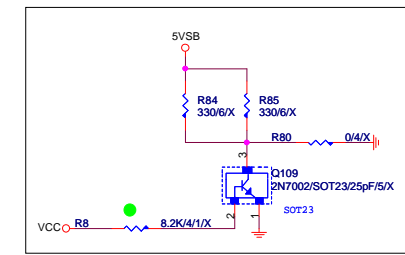
RESET



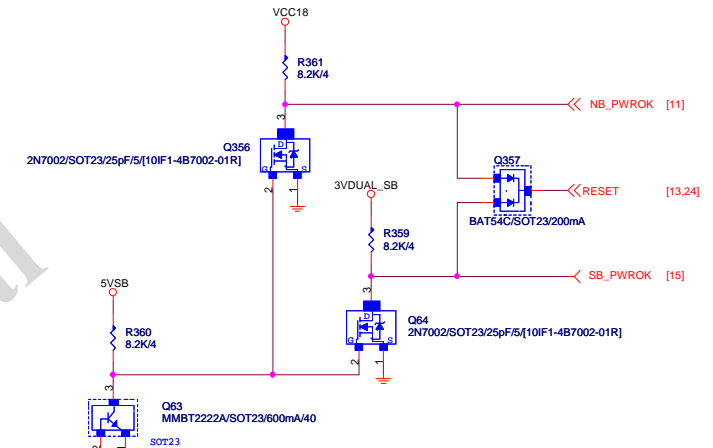
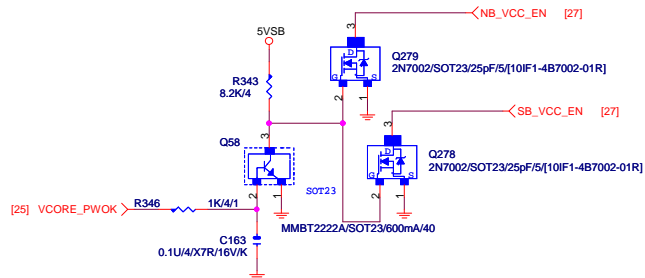
PC SPEAKER



5VSB MiniLoad

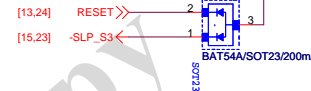


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|----------------------------------|---|--------------------|
| GIGABYTE™ | | |
| Title ATX, FRONT PANEL | | |
| Size Custom | Document Number GA-78LMT-USB3 | Rev 6.01 |
| Date Friday, October 31, 2014 | Sheet 24 | of 31 |

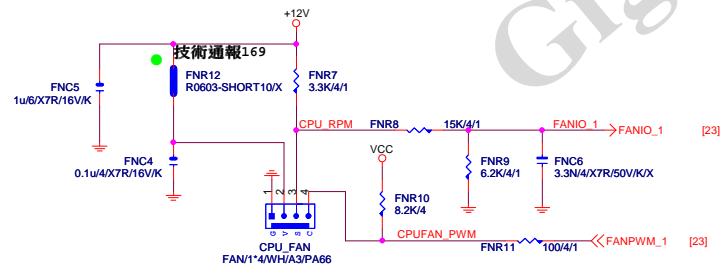


PWOK > NB_PWRGD / SB_PWRGD

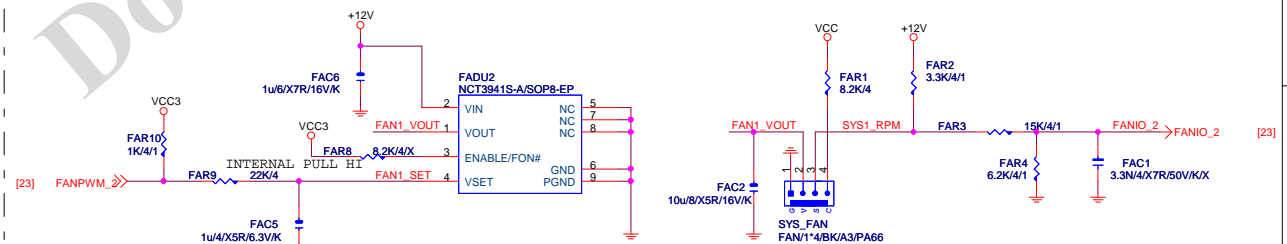
(1.8V , 1.2V , 1.1V) > NB_PWRGD 前 1ms



CPU_FAN PWM Mode

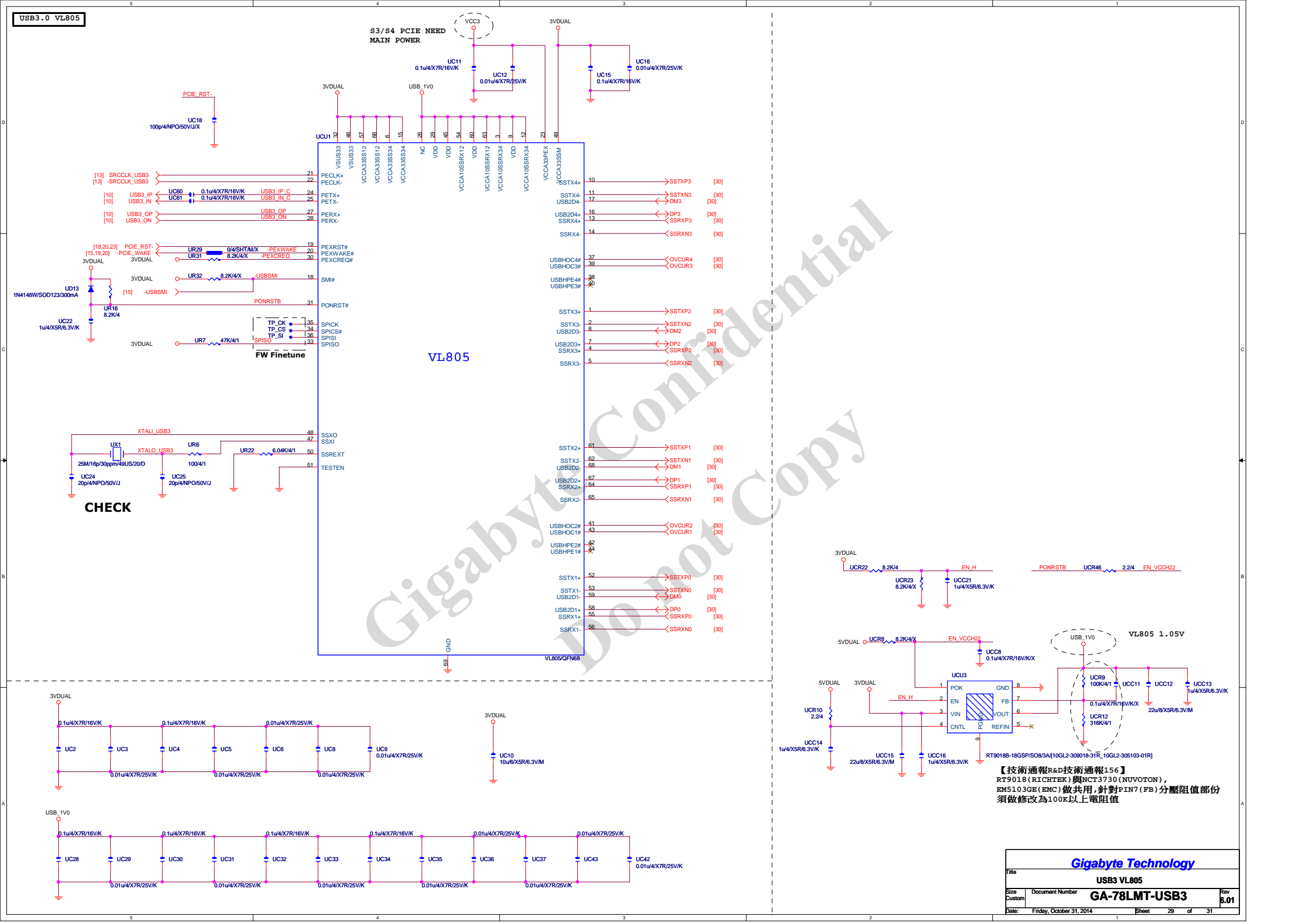


SYS_FAN Voltage Mode

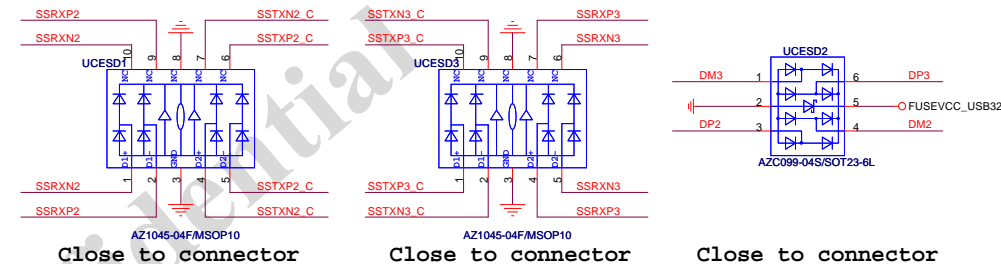
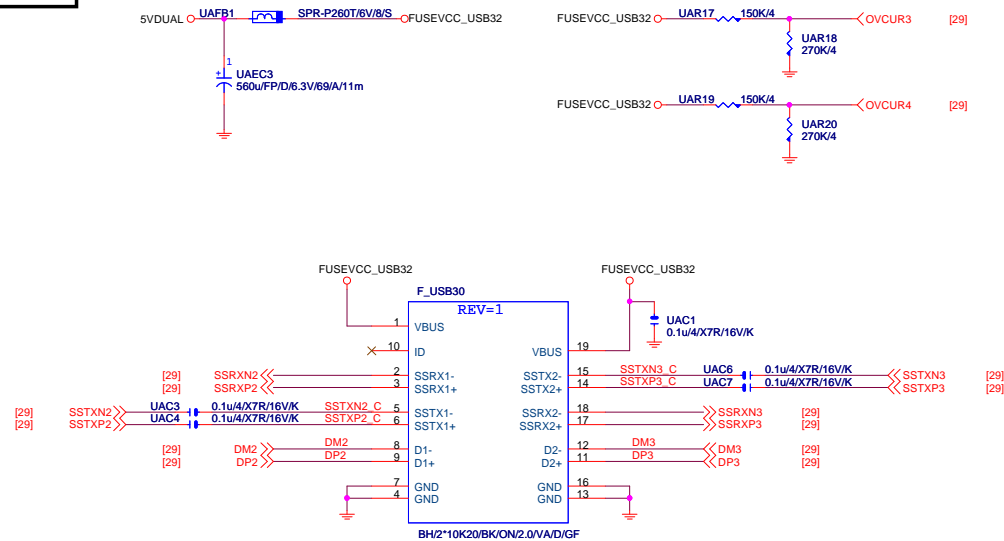


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| Title | | |
|----------------------------|--------------------------|----------------|
| PWR Sequence & CPU/SYS_FAN | | |
| Size | Document Number | Rev |
| Custom | GA-78LMT-USB3 | 6.01 |
| Date: | Friday, October 31, 2014 | Sheet 26 of 31 |



F_USB30



R_USB30

